BEE 332 Devices and Circuits II
Spring 2017
Lab 3: Multi-transistor circuits*

1 Objectives

The objectives of this experiment are to examine the operating characteristics of several of the most common multi-transistor configurations, including current mirrors and differential amplifiers.

2 Circuits

Here are the circuits you'll be experimenting with in this lab.

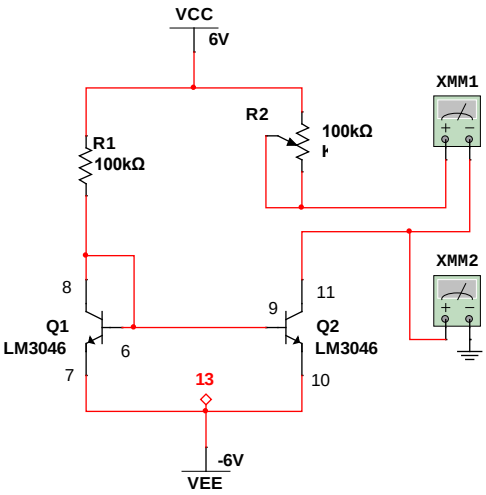


Figure 1. Current mirror.

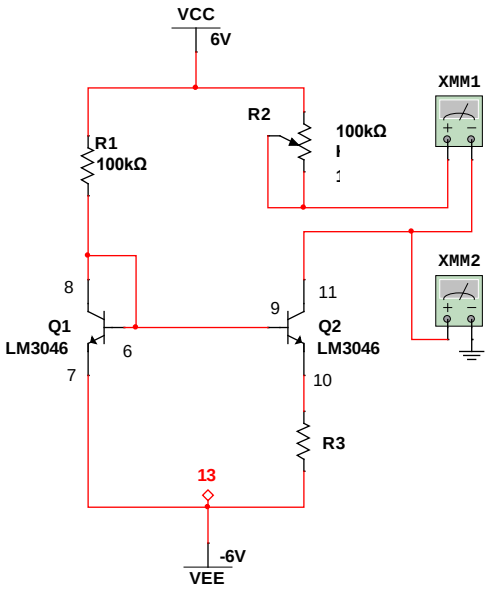


Figure 2. Widlar reducing current source.

* This lab was originally designed by R. B. Darling and has been revised by R. Yotter, T. Chen and N. Hamilton.

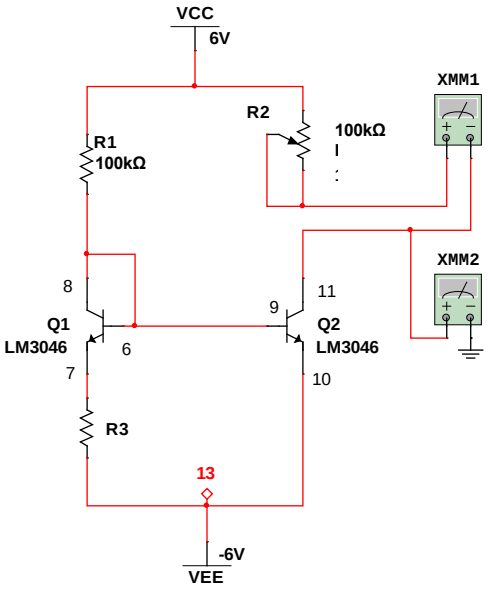


Figure 3. Widlar boosting current source.

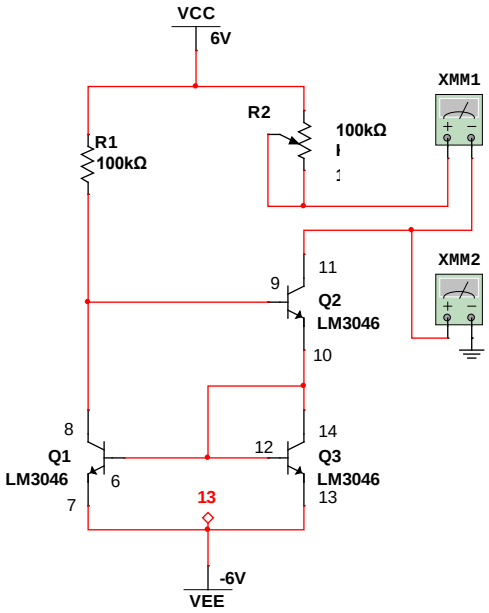


Figure 4. Wilson current source.

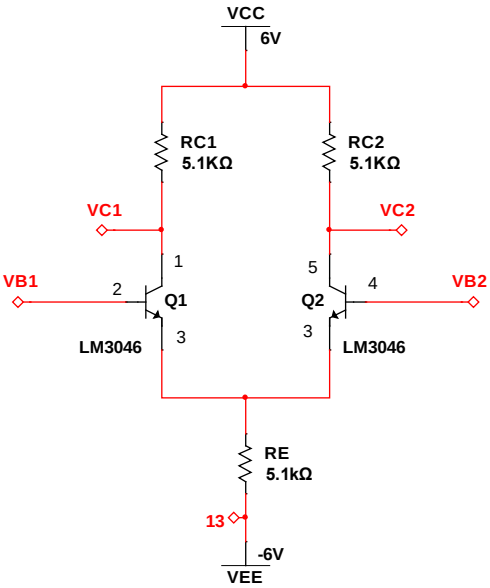


Figure 5. Differential amplifier.

2.1 The LM3046

The National Semiconductor LM3046, shown here in figure 6, also available from other vendors as a CA3046, is an integrated circuit comprised of five *npn* BJTs. The first two are tied together with a common emitter (pin 3), and the last one has its emitter tied to a common *p*-type substrate (pin 13).

The datasheet reports β = 110 typical. Since all five BJTs are fabricated on the same piece of silicon, their characteristics will be very closely matched.

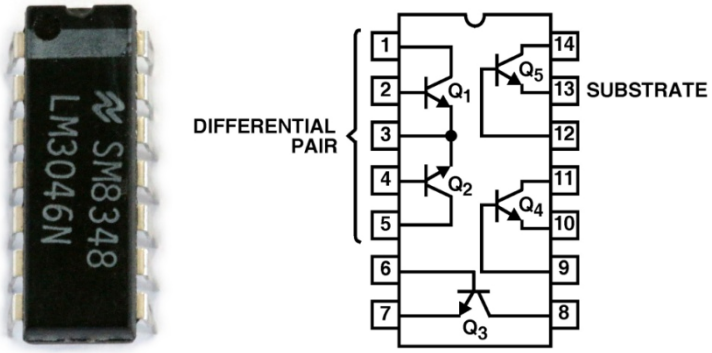
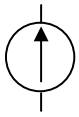


Figure 6. LM3046N package and pinout.
Pinout image source: Intersil CA-3046 datasheet

Since all five BJTs have their collectors embedded in the same substrate, all of the collector-substrate *pn*-junctions must be reverse biased to keep the individual transistors electrically isolated. The substrate on pin 13 MUST be tied to the lowest potential in the circuit, even if the fifth transistor is not being used. Any circuits using the fifth BJT of the LM3046 array MUST tie the emitter of this transistor to the lowest potential power supply rail. Failure to tie pin 13 to the lowest circuit potential will result in very unpredictable behavior.

3 Current sources, sinks and mirrors



A common need in circuit design is to establish a constant DC current for purposes of biasing a transistor, injecting a current offset, or driving a load at a constant current. Constant currents are established by current mirrors, current sinks, and current sources, all of which are often collectively referred to as current sources.

Current *mirrors* replicate an existing current. Current *sinks* pull a fixed current into a node. Current *sources* push a fixed current out of a node.

All of these are based upon the forward active output characteristics of a BJT which provide a controllable current with a typically high value of output resistance, like an ideal current source should.

The simplest description of a BJT is that the collector current is related to the base-emitter voltage as follows, where I_S and V_T are constants.

$$I_C = I_S e^{\frac{V_{BE}}{V_T}}$$

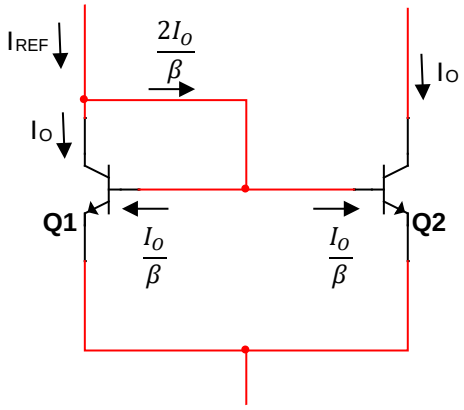


Figure 7. Transistors in parallel.

A current mirror is based upon the idea of keeping the base-emitter voltages of two BJTs identical, by connecting them in parallel as shown in figure 7, thus forcing the collector currents to be identical so long as both are operated in the forward active mode. A reference current is established through one transistor and the second transistor "mirrors" that current into an arbitrary load attached to its collector.

3.1 Circuit

Build the current mirror shown in figure 8 (same as figure 1) using either two multimeters or one multimeter and the oscilloscope. One multimeter should be in series with the R2 potentiometer to measure IC2, the current flowing into the collector of Q2. Use a second multimeter or the oscilloscope to measure VC2, the voltage at the collector of Q2 relative to the system ground.

Record the measured values for your resistors, power supplies and VB1, the base voltage of Q1.

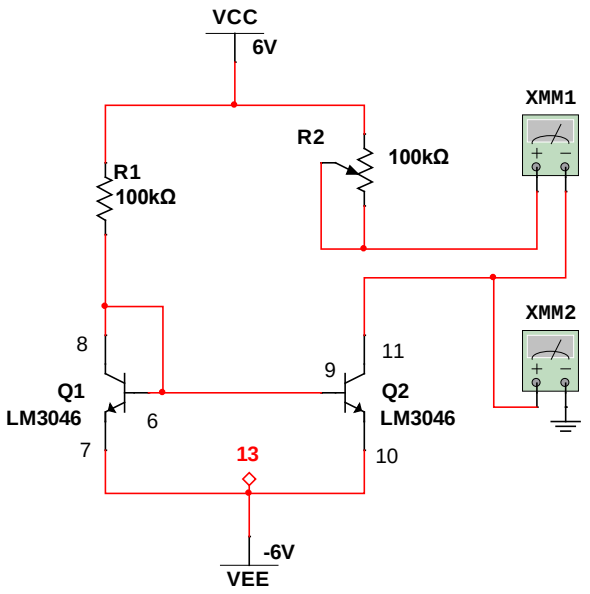


Figure 8. Current mirror.

3.2 Measurements

An ideal current source will keep the current constant, independent of the load conditions.

To determine the ideality of this current source, create a table of measurements of VC2, the collector voltage of Q2, versus IC2, the collector current, as you adjust R2, simulating a varying load. Vary VC2 from +6.0 V down to about -5.0 V in 1.0 V steps, as closely as you can.

VC2 (V)	IC2 (μA)
6.0	
5.0	
4.0	
:	
-4.0	
-5.0	

Keep this circuit set up as is. It will be only slightly modified in the following procedures.

3.3 Analysis

1. Calculate IC1 assuming β = 110.
2. Plot IC2 versus VC2 with VC2 on the X-axis.
3. Calculate the output resistance of this current source, $Rout = \frac{\Delta V}{\Delta I}$.
4. Explain what purpose the connection between the base and collector of Q1 (pins 6 and 8) serves.

5. Explain why the collector voltage of Q2 cannot be brought all of the way down to the lower power supply rail of VEE = -6.0 V.
6. Explain if and how the current source is sensitive to the values of the power supply voltages.
7. Design a new current source for which the output current is exactly twice that of the reference current by using three of the BJTs on the LM3046 *npn* array. Explain how this circuit achieves the factor of two scaling between the reference and output currents.

4 Widlar reducing source

If a resistor is placed in series with the emitter of one of the two transistors of a current mirror, the base-emitter voltages will no longer be equal and the currents through the two transistors are scaled relative to one another. This is the principle of the Widlar current source in which the reference current can be either scaled down or scaled up.

4.1 Circuit

In this first variation, shown in figure 9 (same as figure 2), R3 is placed in series with the emitter of Q2. The voltage drop across R3 makes VBE2 < VBE1, causing IC2 < IC1. This is the reducing Widlar current source.

The value of R3 to obtain a specific current from the Widlar current source is given as

$$R3 = \frac{V_T \ln\left(\frac{IC1}{IC2}\right)}{IC2}$$

1. Derive this equation starting from

$$I_C = I_S e^{\frac{V_{BE}}{V_T}}$$

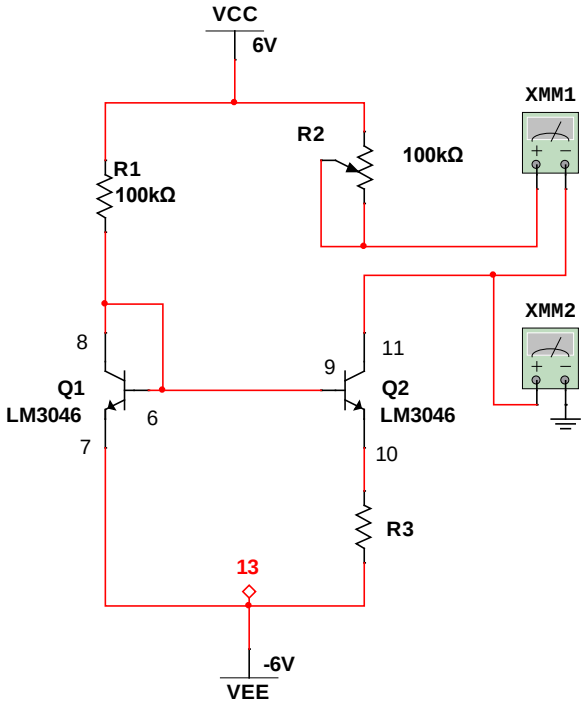


Figure 9. Widlar reducing source.

2. Calculate the value of R3 for this Widlar current source to produce IC2 = 10 µA. You may assume IC1 is the same as you measured in the previous procedure. You should obtain a value in the range of 5 to 10 KΩ. Choose the closest value you have in your kit.
3. Build this circuit and record measured values for your resistors, power supplies and VB1.

4.2 Measurements

Create a table of measurements of VC2, the collector voltage of Q2, versus IC2, the collector current, as you adjust R2, simulating a varying load. Vary VC2 from +6.0 V down to about 5.0 V in 0.1 V steps, as closely as you can.

Because a smaller current now flows through the potentiometer R2, it will only allow VC2 to be adjusted downward by about 1.0 V.

VC2 (V)	IC2 (µA)
6.0	
5.9	
5.8	
:	
5.1	
5.0	

4.3 Analysis

1. Plot IC2 versus VC2 with VC2 on the X-axis.
2. Calculate the output resistance of this current source, $Rout = \frac{\Delta V}{\Delta I}$.

5 Widlar boosting source

In this second variation, shown in figure 10 (same as figure 3), R3 is placed in series with the emitter of Q1. The voltage drop across R3 makes VBE2 > VBE1, causing IC2 > IC1. This is the boosting Widlar current source.

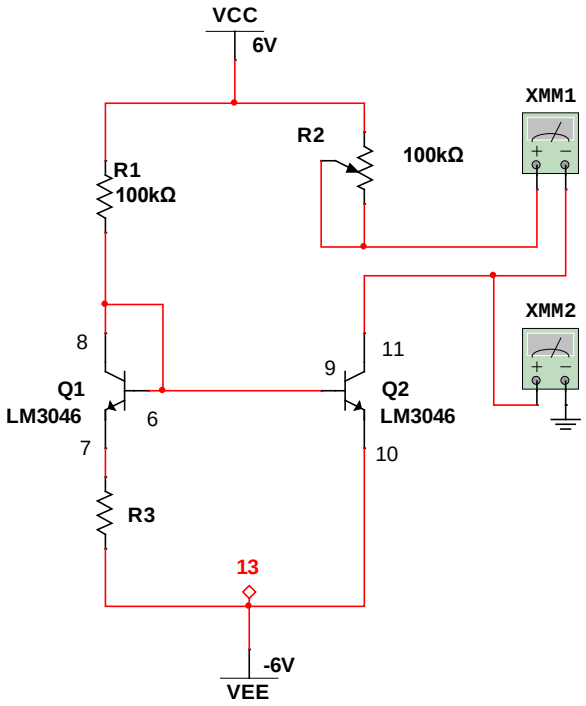


Figure 10. Widlar boosting source.

5.1 Circuit

The value of R3 to obtain a specific current from the Widlar current source is given as

$$R3 = \frac{V_T \ln\left(\frac{IC2}{IC1}\right)}{IC1}$$

1. Calculate the value of R3 for this Widlar current source to produce IC2 = 1.0 mA. You may assume IC1 is the same as before. You should obtain a value in the range of 400 to 600 Ω. Choose the closest value you have in your kit.
2. Build this circuit and record measured values for your resistors, power supplies and VB1.

5.2 Measurements

Create a table of measurements of VC2, the collector voltage of Q2, versus IC2, the collector current, as you adjust R2, simulating a varying load.

Adjust the R2 potentiometer to vary the collector voltage of Q2 from +6.0 V down -5.0 V in 1.0 V steps until IC2 suddenly falls. Because a larger current now flows through the potentiometer R2, IC2 can be increased to the point where Q2 saturates. Once this occurs, the output current falls precipitously.

VC2 (V)	IC2 (µA)
6.0	
5.0	
4.0	
:	
-4.0	
-5.0	

5.3 Analysis

1. Plot IC2 versus VC2 with VC2 on the X-axis.
2. Calculate the output resistance of this current source, $Rout = \frac{\Delta V}{\Delta I}$.
3. Explain why the output resistance of the reducing Widlar current source is higher than for the boosting case.

6 Wilson current source

The output resistance of a current source is strong function of the resistance is in series with the emitter of the output transistor.

6.1 Circuit

One way to increase the output resistance and thus creating a more ideal current source is to stack two or more transistors as shown in figure 11 (same as figure 4). The output resistance of the bottom transistor is then amplified by the ones on top of it. This is the principle of the Wilson current source.

Build this circuit and record measured values for your resistors, power supplies and VB1.

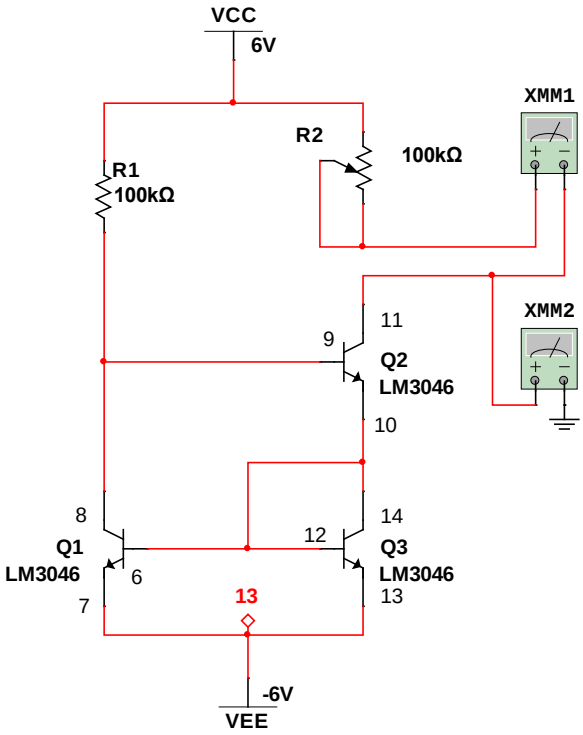


Figure 11. Wilson current source.

6.2 Measurements

Create a table of measurements of VC2, the collector voltage of Q2, versus IC2, the collector current, as you adjust R2, simulating a varying load.

Adjust the R2 potentiometer to vary the collector voltage of Q2 from +6.0 V down -5.0 V in 1.0 V steps.

VC2 (V)	IC2 (μA)
6.0	
5.0	
4.0	
:	
-4.0	
-5.0	

6.3 Analysis

1. Plot IC2 versus VC2 with VC2 on the X-axis.
2. Calculate the output resistance of this current source, $Rout = \frac{\Delta V}{\Delta I}$.

7 Differential amplifier

A differential amplifier, as shown in figure 12 (same as figure 5), is designed to amplify the difference between two input voltages and reject the average between the two input voltages.

The difference between two signals is termed the differential-mode signal, while the arithmetic average of two signals is termed the common-mode signal.

The common-mode rejection ratio (CMRR) is the differential-mode gain divided by the common-mode gain.

If only one side of the input or output is used, that input or output is termed *unbalanced*, single-ended or unipolar.

A balanced signal is a pair of signals whose magnitudes are the same but whose polarities are opposite.

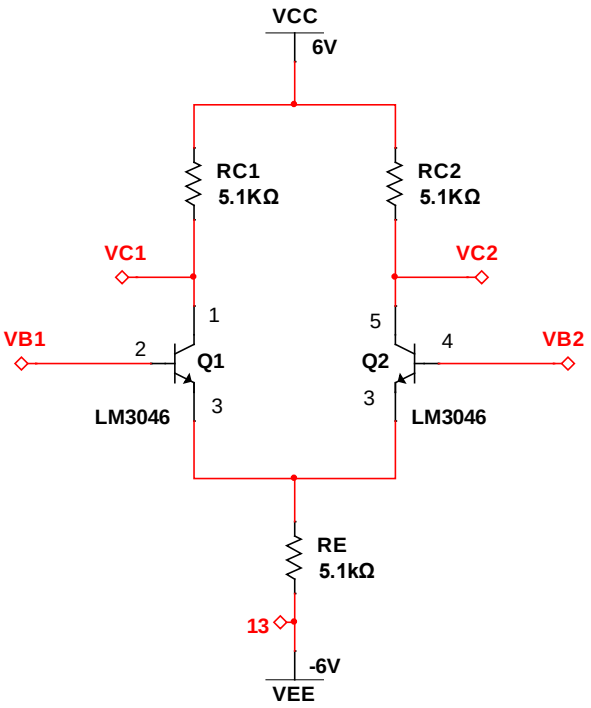


Figure 12. Differential amplifier.

If both sides of the input or output are used, it's termed *balanced*, double-ended, or bipolar input or output.

7.1 Grounded inputs

Build the circuit in figure 12, grounding both VB1 and VB2 as shown in figure 13. Record measured values for your resistors and for VC1, VC2 and VE1 = VE2.

Verify that both Q1 and Q2 are in the forward active region. Voltages on the collectors of both Q1 and Q2 should be around +3 V. If this is not the case, identify and fix the problem before proceeding further.

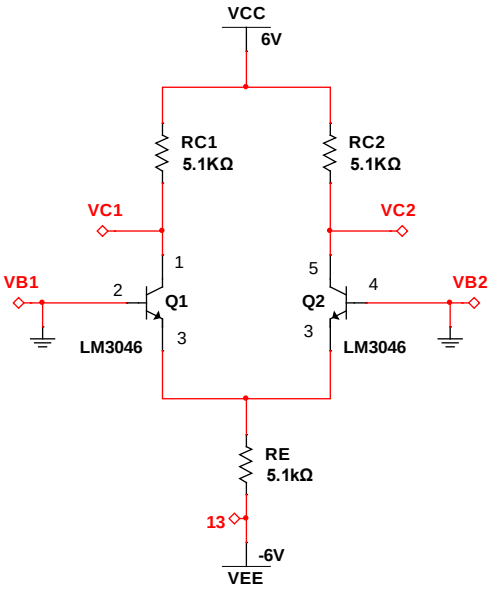


Figure 13. Grounded inputs.

7.2 Differential mode

Reconfigure the circuit as shown in figure 14 with Vin = 100 mVpp, 1 KHz sine wave, 0 V DC offset applied to VB1 and with VB2 still grounded.

1. Capture oscilloscope screenshots with Vin on channel 1 and VC1 on channel 2 and then again with VC2 on channel 2 with on-screen measurements of frequency and the peak-to-peak input and output voltages. Use AC coupling on channel 2 to subtract out the DC bias. Note the polarity of the output relative to the input. You should observe that VC1 and VC2 are the same amplitude but inverted.
2. Calculate the differential mode gain, Av, in each case by dividing the amplitude of the output by the amplitude of the input. This is the gain from a *single-ended input* to a *single-ended output:* The input signal was applied to the base of only one transistor and the base of the other was grounded. A double-ended input would have applied the opposite signal to VB2. Similarly, the output was taken from only one of the collectors. A double-ended output would have been taken from between the two collectors.

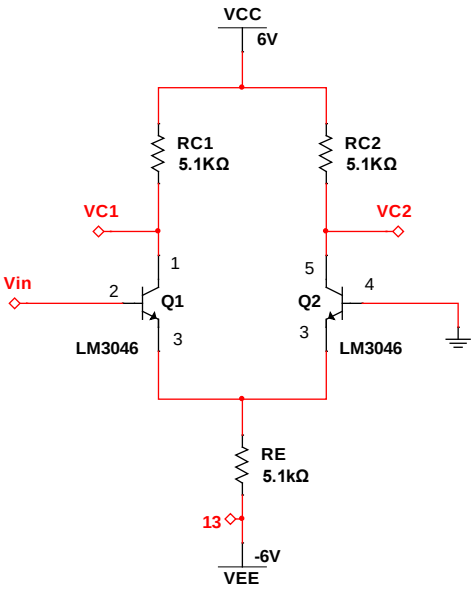


Figure 14. Differential mode.

3. Increase the frequency of Vin until Av has fallen by 3 dB. Capture a screenshot and calculate Av.

7.3 Common mode

Reconfigure the circuit as shown in figure 15, with Vin = 3.0 Vpp, 1 KHz sine wave, 0 V DC offset. This will apply a common-mode input signal to the differential amplifier from which the common-mode gain can be determined.

1. Capture screenshots of Vin versus VC1 and Vin versus VC2, again with on-screen measurements and with AC coupling on channel 2. Note the polarity of the output relative to the input. You should observe that VC1 and VC2 are the same.
2. Calculate the common mode voltage gain, Av.
3. Increase the frequency of Vin until Av has fallen by 3 dB. Capture a screenshot and calculate Av.
4. Reset Vin = 200 mVpp, 1 KHz, +4.9 V DC offset. Capture screenshots using both AC and DC coupling on channel 2.

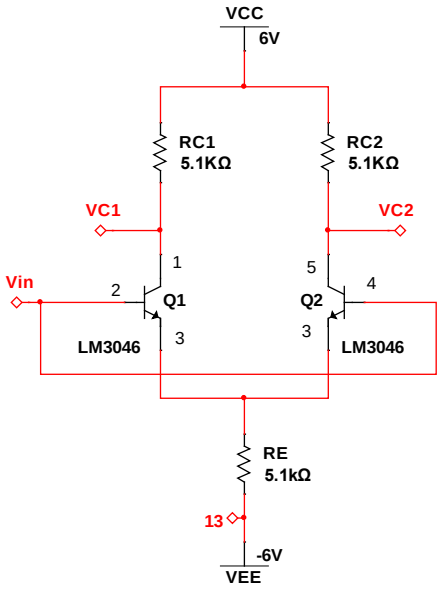


Figure 15. Common mode.

7.4 Analysis

1. Calculate the common-mode rejection ratio (CMRR), expressing it in both as a ratio and in decibels (dB).
2. Explain why the common-mode gain is approximately 0.5 and inverting when no DC offset is applied from the signal generator.
3. Explain why the common-mode gain jumps to approximately 1.0 and becomes non-inverting when a positive DC offset is applied from the signal generator. This is a tricky question! But it represents a situation which often occurs in the lab and which confuses people.
4. Suggest a way to increase the CMRR of this differential amplifier. Hint: think about how ideal the current source RE is and how it might be improved.